

80-CHANNEL SEGMENT DRIVER FOR DOT MATRIX LCD

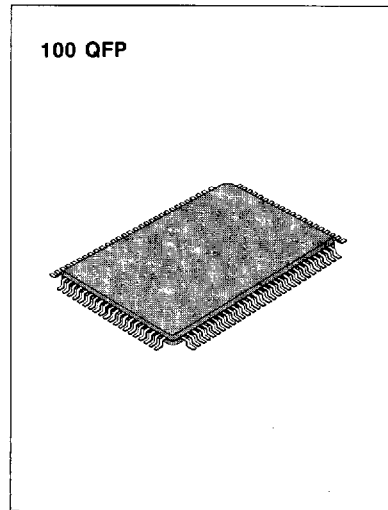
The KS0063 is a LCD driver LSI which is fabricated by low power CMOS technology. Basically this LSI consists of 40x2 bit bidirectional shift register, 40x2 bit data latch and 40x2 bit LCD driver (refer to Fig 1) This LSI can be used segment driver.

FUNCTION

- Dot matrix LCD driver with 80 channel output.
- Input/Output signal
 - output: 40 x 2 channel waveform for LCD driving
 - Input : - Serial display data and control pulse from the controller LSI.
 - Bias voltage (V₁-V₄)

FEATURES

- Display driving bias; static-1/5
- Power supply voltage; +5V ± 10%
- Supply voltage for display: 0~-5V(V_{EE})
- interface



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driver (cascade connection)	controller
KS0065, Other KS0063	KS0066

- CMOS Process
- 100QFP and bare chip available

BLOCK DIAGRAM

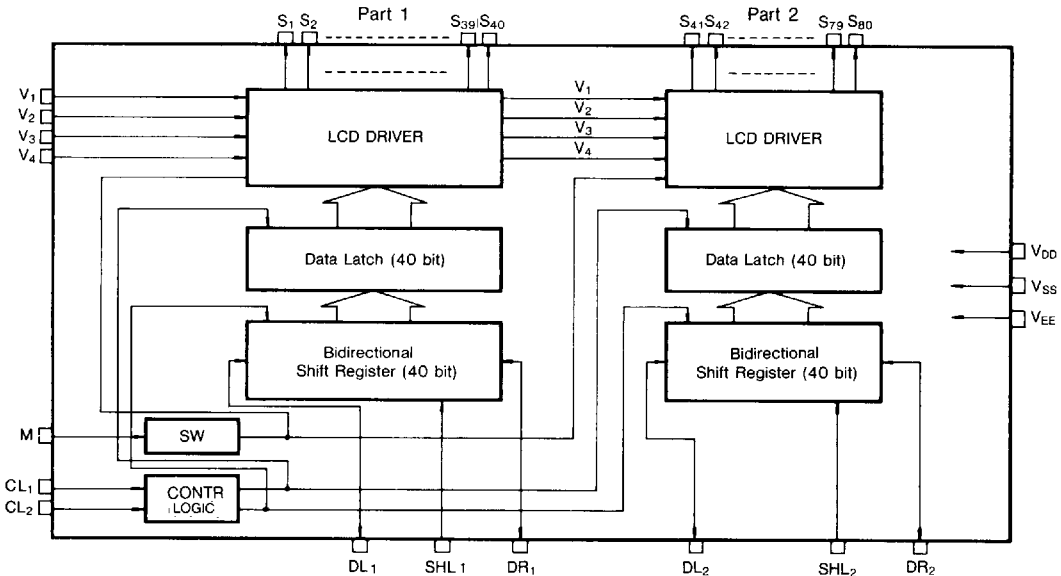


Fig. 1. KS0063 functional block diagram

PIN CONFIGURATION

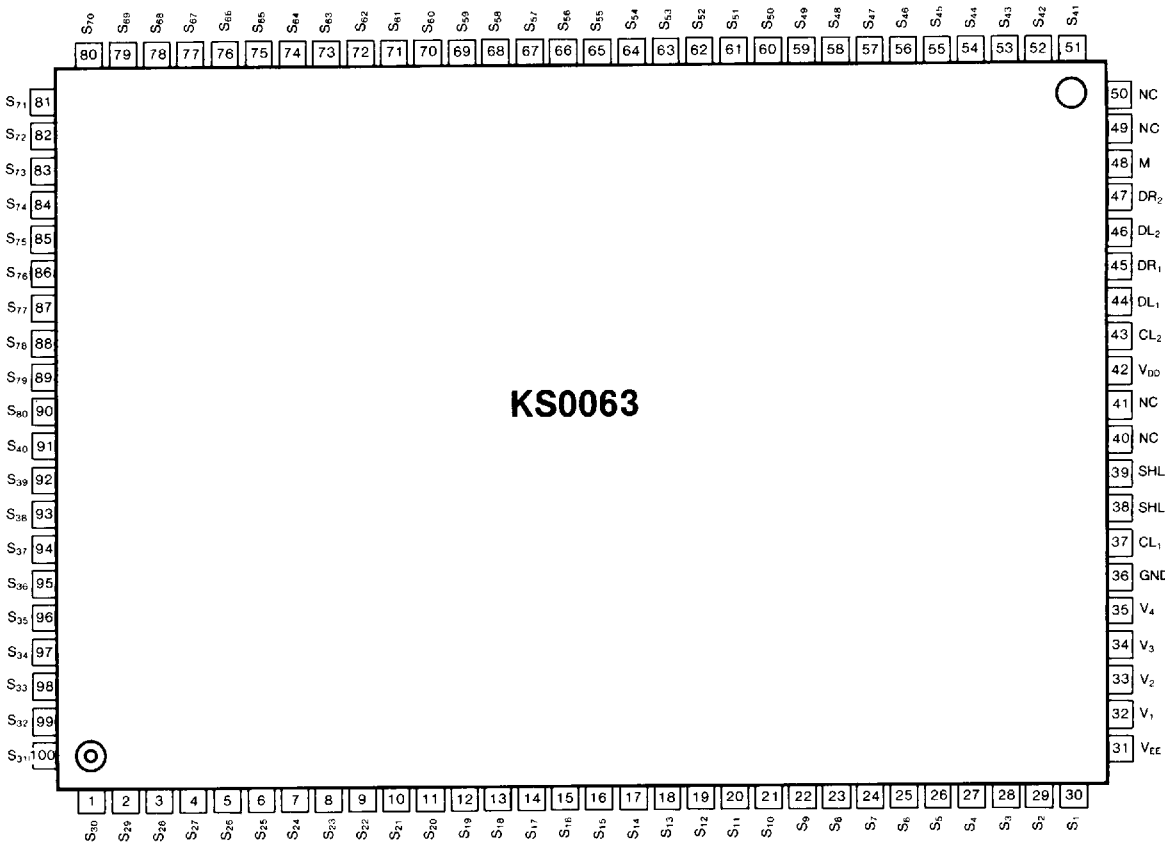


Fig. 2. 100 QFP Top View

PIN DESCRIPTION

PIN (NO.)	INPUT OUTPUT	NAME	DESCRIPTION	INTERFACE										
V _{DD} (42)		Power Supply	For logical circuit (+5V±10%)	Power Supply										
GND(36)			0V (GND)											
V _{EE} (31)			For LCD driver circuit (-5V)											
V1, V2 (32,33)	Input	LCD drive	Bias voltage level for LCD drive (Select level)	Power										
V3, V4 (34,35)	Input		Bias voltage level for LCD drive (Nonselect level)											
S1-S40	Output	LCD driver	LCD driver output	LCD										
SHL1(38)	Input	Part 1	Data Interface	V _{DD} or V _{SS}										
			<table border="1"> <thead> <tr> <th>SHL1</th> <th>DL1</th> <th>DR1</th> </tr> </thead> <tbody> <tr> <td>V_{DD}</td> <td>OUT</td> <td>IN</td> </tr> <tr> <td>V_{SS}</td> <td>IN</td> <td>OUT</td> </tr> </tbody> </table>		SHL1	DL1	DR1	V _{DD}	OUT	IN	V _{SS}	IN	OUT	
SHL1	DL1		DR1											
V _{DD}	OUT	IN												
V _{SS}	IN	OUT												
		Data Input/output of shift register (part 1)												
DL1, DR1 (44,45)	Input Output			Controller or KS0063										
S41-S80	Output	LCD driver	LCD driver output	LCD										
SHL2 (39)	Input	Part 2	Data Interface	V _{DD} or V _{SS}										
			<table border="1"> <thead> <tr> <th>SHL2</th> <th>DL2</th> <th>DR2</th> </tr> </thead> <tbody> <tr> <td>V_{DD}</td> <td>OUT</td> <td>IN</td> </tr> <tr> <td>V_{SS}</td> <td>IN</td> <td>OUT</td> </tr> </tbody> </table>		SHL2	DL2	DR2	V _{DD}	OUT	IN	V _{SS}	IN	OUT	
SHL2	DL2		DR2											
V _{DD}	OUT	IN												
V _{SS}	IN	OUT												
		Data input/output of shift register (part 2)												
DL2, DR2 (46,47)	Input Output			Controller or KS0063										
M(48)	Input	Alternated signal for LCD driver output		Controller										
CL1, CL2 (37,43)	Input	Data shift/latch clock	CL1: Data latch clock CL2: Data shift clock											
NC (40,41,49,50)			No connection	NC										

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MAXIMUM ABSOLUTE LIMIT (Ta=25°C)

Characteristic	Symbol	Value	Unit
Power supply Voltage	V _{DD}	-0.3~+7.0	V
Driver Supply Voltage	V _{LCD}	V _{DD} -13.5~V _{DD} +0.3	V
Input Voltage 1	V _{IN1}	-0.3~V _{DD} +0.3	V
Input Voltage 2 (V ₁ -V ₄)	V _{IN2}	V _{DD} +0.3~V _{EE} -0.3	V
Operating Temperature	T _{opr}	-20~+75	°C
Storage temperature	T _{stg}	-55~+125	°C

*Voltage greater than above may damage to the circuit

*V_{EE}: connect a protection resistor (220Ω ±5%)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD}=+5V±10% V_{EE}=-5±10% V_{SS}=0V, Ta=25°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Supply current	I _{DD}	f _{CL2} =400kHz	—	1	mA	
	I _{EE}	f _{CL1} =1KHz	—	10	μA	
Input Voltage	V _{IH}	—	0.7V _{DD}	V _{DD}	V	CL1, CL2, DL1 DL2, DR1, DR2 SHL1, SHL2, M,
	V _{IL}		0	0.3V _{DD}		
Input leakage current	I _{IL}	V _{IN} =0~V _{DD}	-5	5	μA	
Output Voltage	V _{OH}	I _{OH} =-0.4mA	V _{DD} -0.4	—	V	DL1, DL2, DR1, DR2
	V _{OL}	I _{OL} =+0.4mA	—	0.4		
Voltage descending	V _{d1}	I _{ON} =0.1mA for one of S ₁ -S ₈₀	—	1.1	V	V(V ₁ -V ₄)-S(S ₁ -S ₈₀)
	V _{d2}	I _{ON} =0.05mA for each S ₁ -S ₈₀	—	1.5		
Leakage current	I _{V1}	V _{IN} =V _{DD} ~V _{EE} (Output S ₁ ~S ₈₀ : floating)	-10	10	μA	V ₁ -V ₄

AC CHARACTERISTICS (V_{DD}=5V±10%, V_{EE}=-5V±10%, V_{SS}=0V, Ta=25°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data shift frequency	f _{CL}	—	—	400	KHz	CL2
Clock High level width	t _{CWH}	—	800	—	ns	CL1, CL2
Clock low level width	t _{CWL}	—	800	—		CL2
Clock set-up time	t _{SL}	from CL2 to CL1	500	—		CL1, CL2
	t _{LS}	from CL1 to CL2	500	—		
Clock rise/fall time	t _{CT}	—	—	200		DL1, DL2, DR1, DR2
Data Set-up time	t _{SU}	—	300	—		
Data hold time	t _{DH}	—	300	—		
Data delay time	t _{PD}	CL=15PF	—	500		

TIMING CHARACTERISTICS

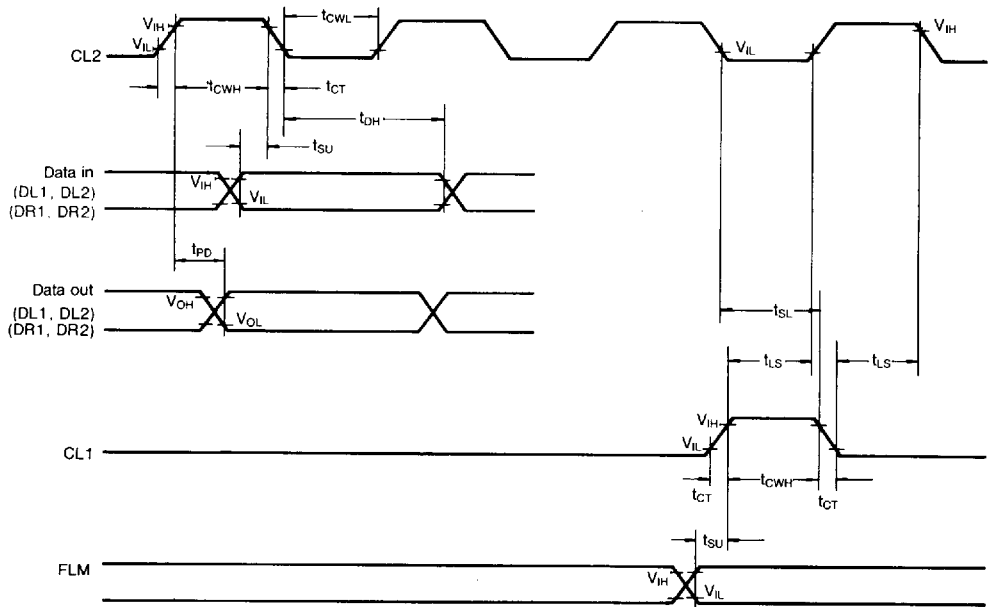
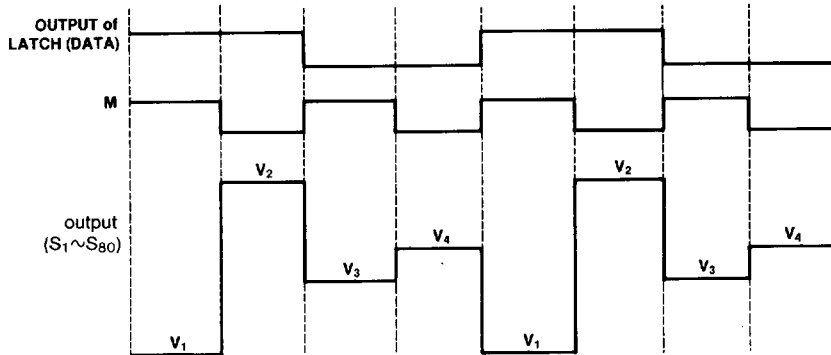


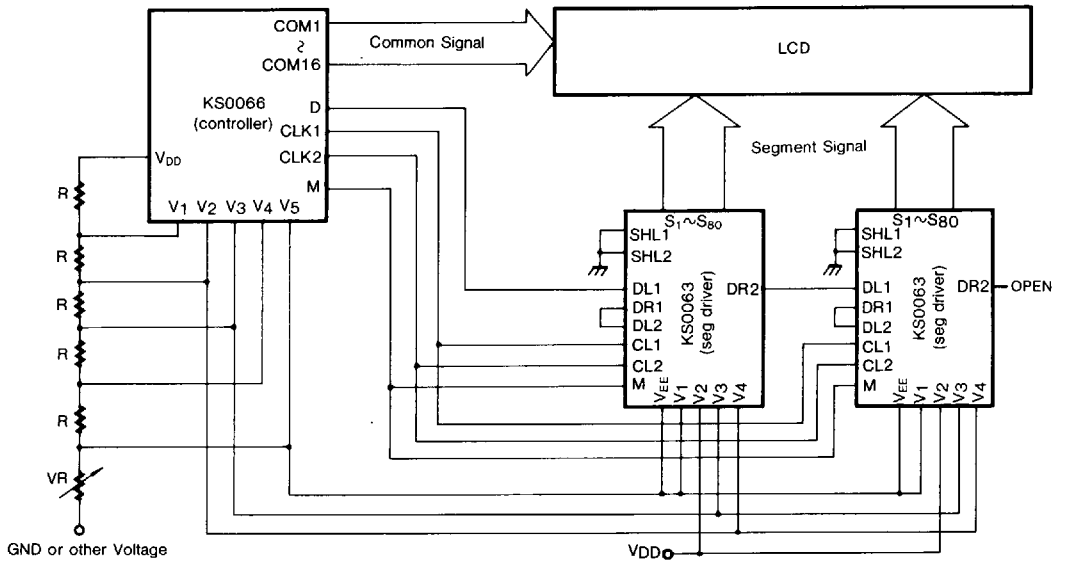
Fig. 3. AC characteristics

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LCD OUTPUT WAVEFORMS



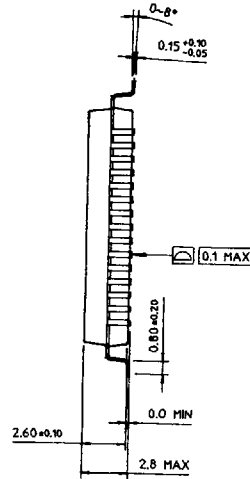
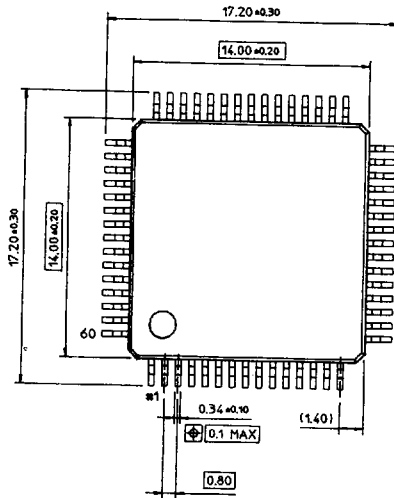
APPLICATION CIRCUIT



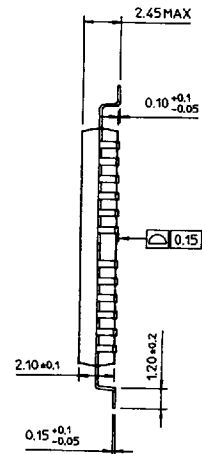
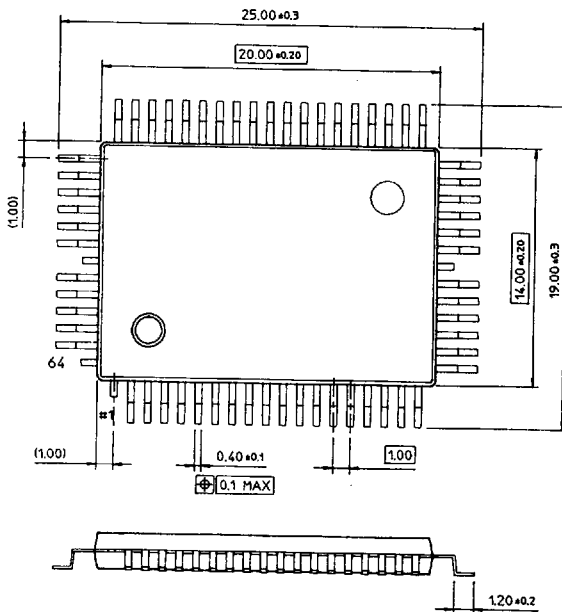
PACKAGE DIMENSIONS

Dimensions in Millimeters

60-QFP-1414A



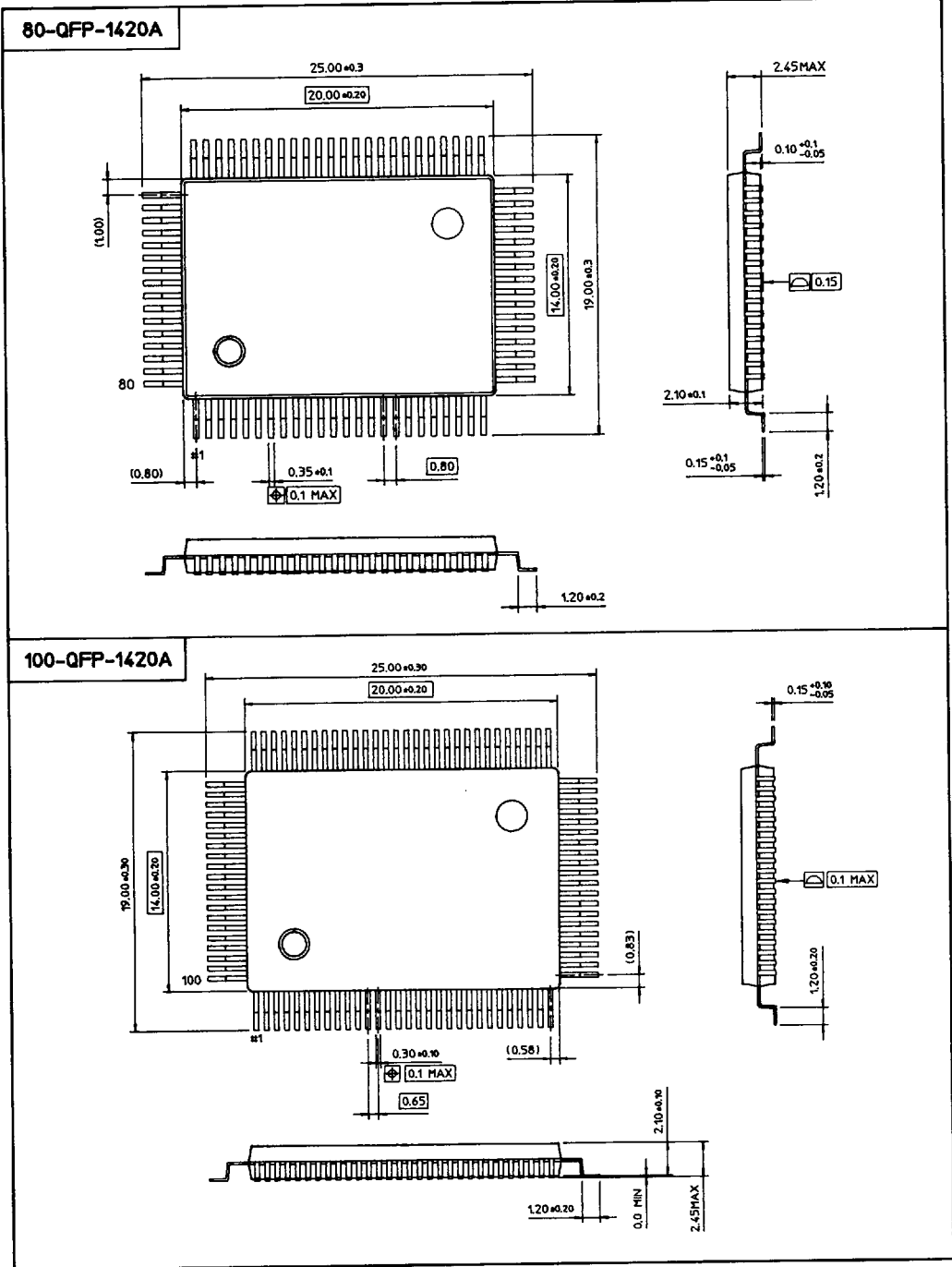
64-QFP-1420D



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PACKAGE DIMENSIONS

Dimensions in Millimeters

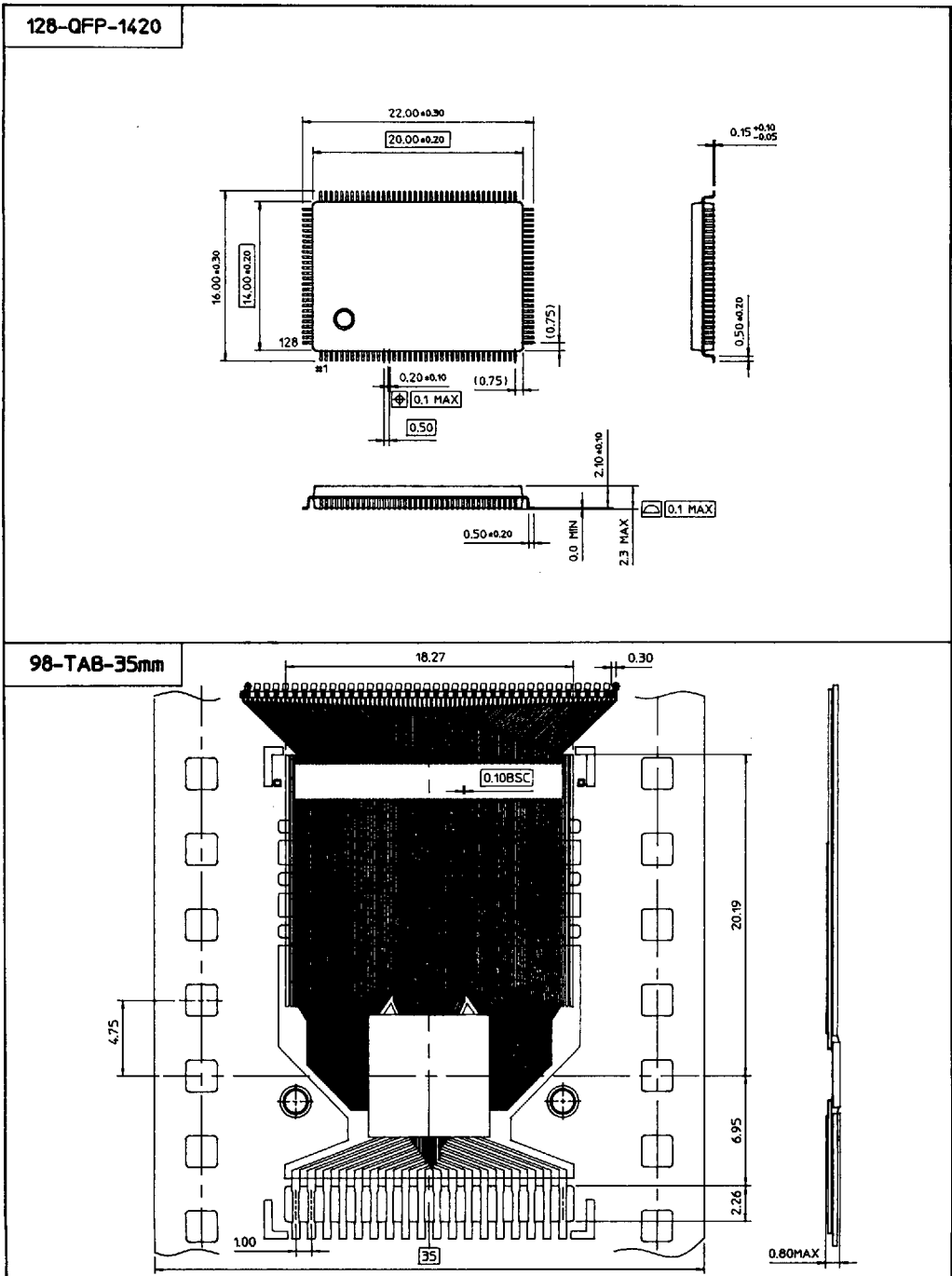


ELECTRONICS

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PACKAGE DIMENSIONS

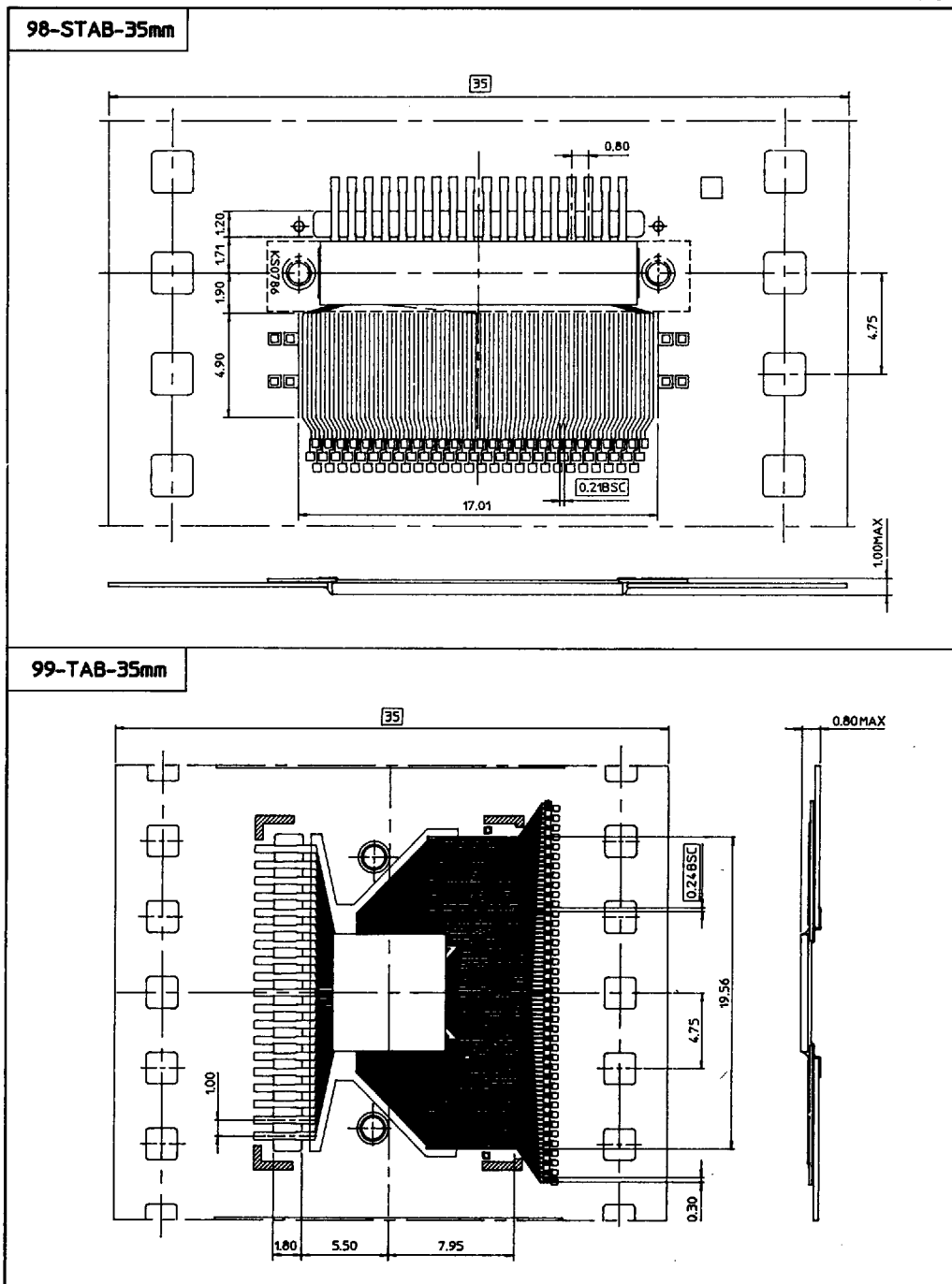
Dimensions in Millimeters



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PACKAGE DIMENSIONS

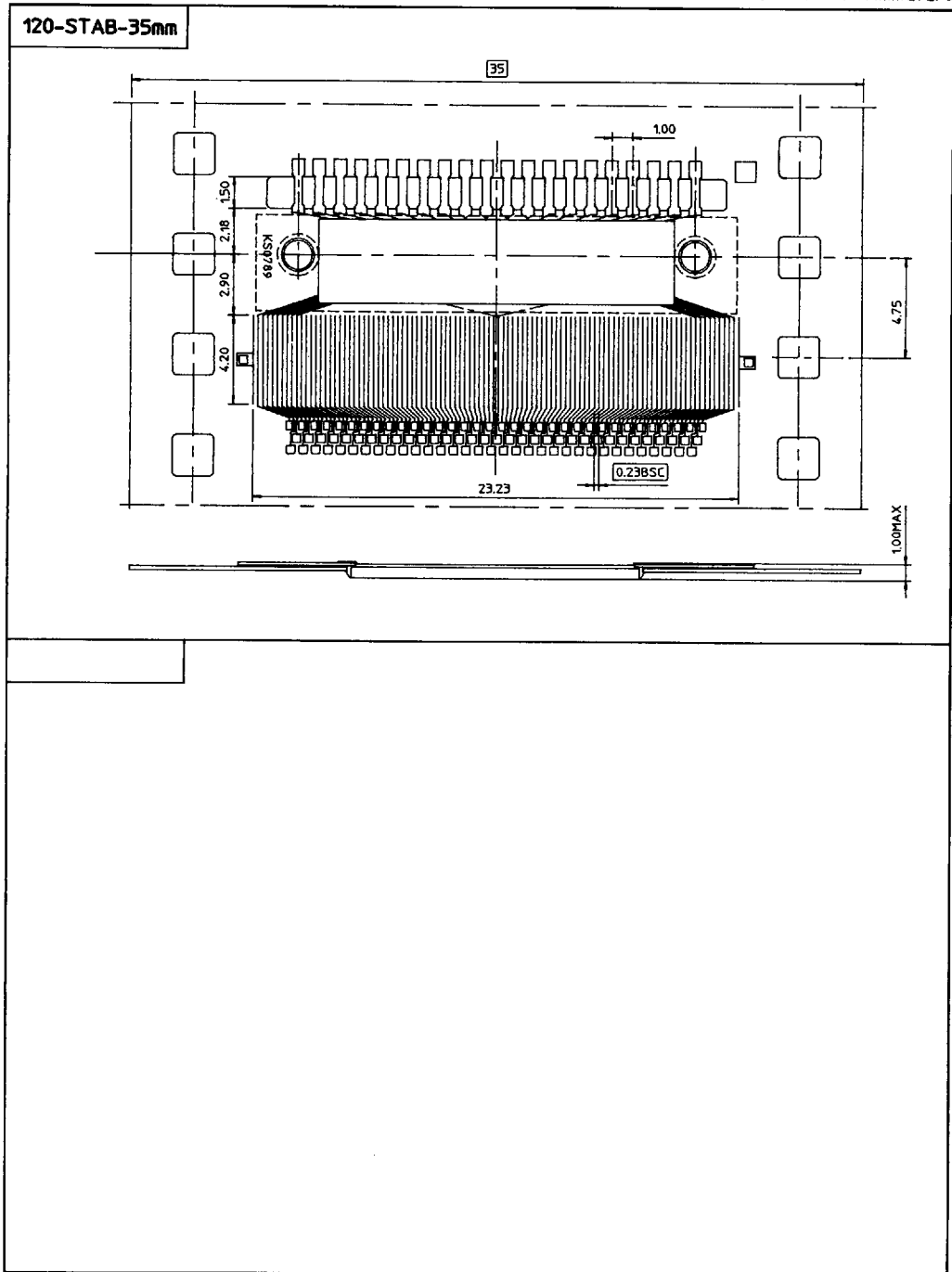
Dimensions in Millimeters



ELECTRONICS

PACKAGE DIMENSIONS

Dimensions in Millimeters



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